

Synchronous Sequential Logic

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Sequential Circuits

- Outputs are function of inputs and present states
- Present states are supplied by memory elements

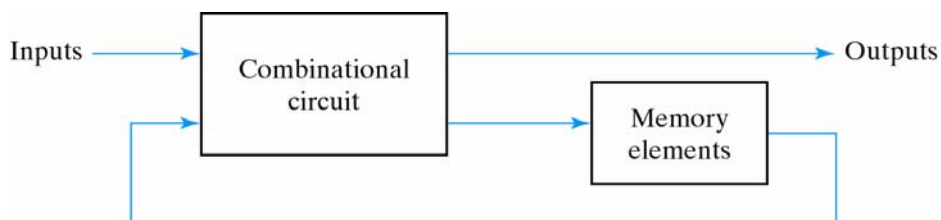


Fig. 5-1 Block Diagram of Sequential Circuit

Sequential Circuits

- Two types of sequential circuit
 - Synchronous : behavior depends on the signals affecting storage elements at discrete time
 - Asynchronous : behavior depends on inputs at any instance of time, many difficulties on designers
- Flip-flop: The storage elements used in clocked sequential circuits.

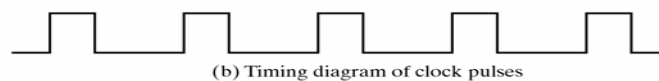
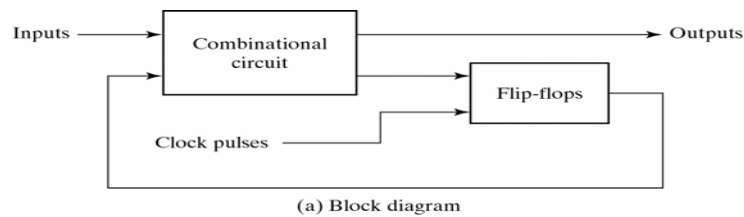


Fig. 5-2 Synchronous Clocked Sequential Circuit

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Latches

- The most basic types of flip-flops operate with signal levels
- The latches introduced here are the basic circuits from which all flip-flops are constructed
- Useful for
 - Storing binary information
 - For the design of asynchronous sequential circuits
- Not practical for use in synchronous sequential circuits

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SR Latch

- Consist of two cross-coupled NOR gates
 - $S=1, R=0$ then $Q=1$ (set)
 - $S=0, R=1$ then $Q=0$ (reset)
 - $S=0, R=0$ then no change (keep condition)
 - $S=1, R=1$ $Q=Q'=0$ (undefined)

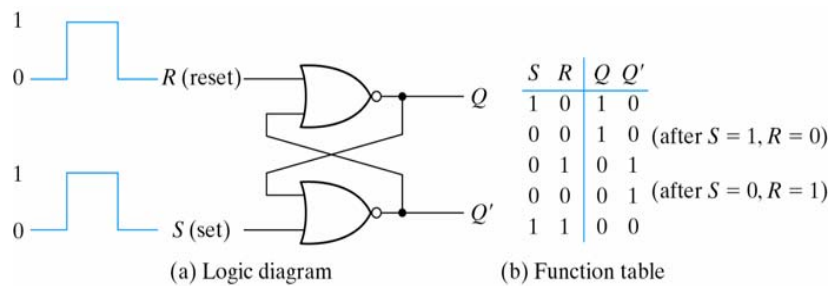


Fig. 5-3 SR Latch with NOR Gates

S'R' Latch with NAND Gates

- Require the complement value of NOR latch

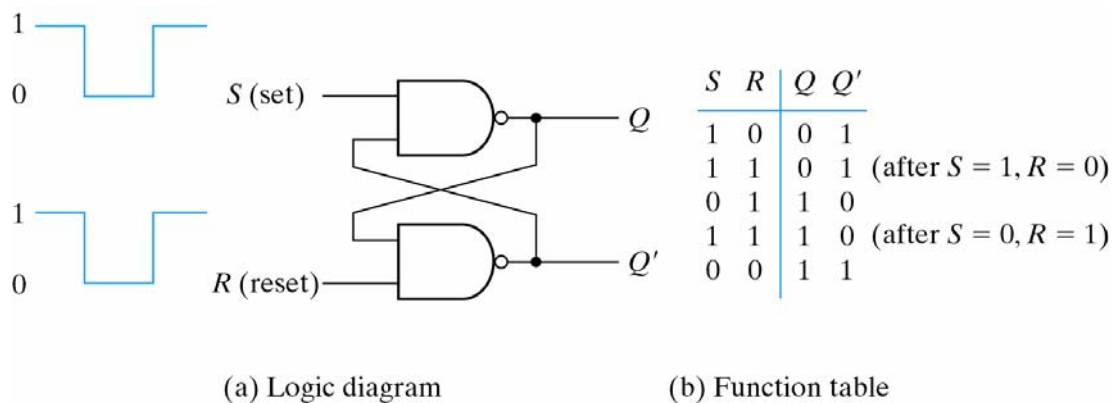
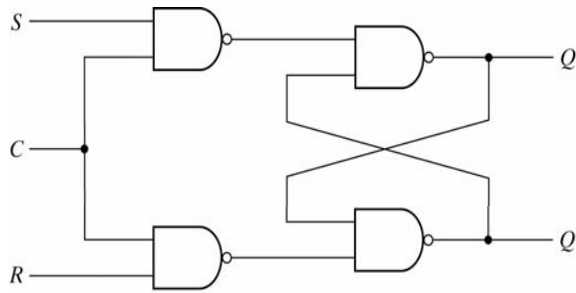


Fig. 5-4 SR Latch with NAND Gates

SR Latch with Control Input

- Add two NAND gate and control signal
- $C=0$ (no action), $C=1$ (act as SR latch)



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

SR Latch as a Debouncing Switch

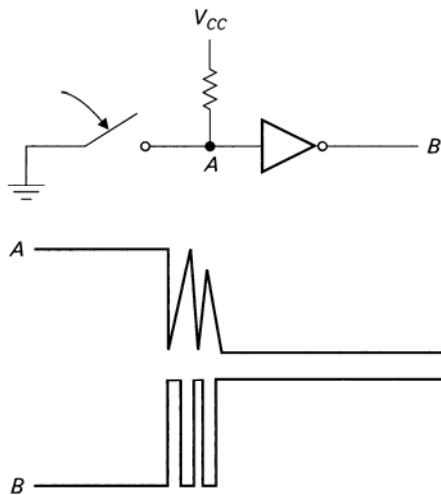


FIGURE 7-16 Switch bounce

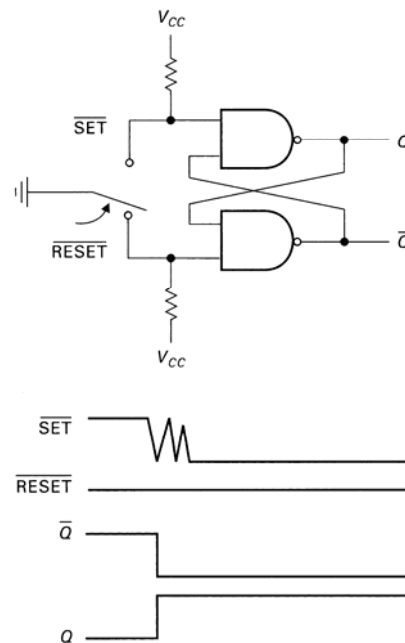
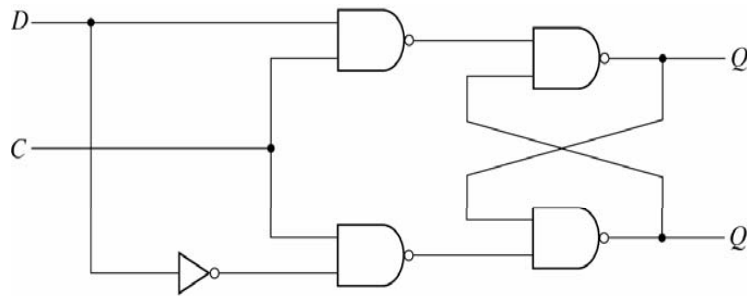


FIGURE 7-17 SET-RESET flip-flop used as a debounce switch

D Latch

- Eliminate indeterminate state in SR latch
- $C=1$, output value is equal to D (*transparent*)



C	D	Next state of Q
0	X	No change
1	0	$Q = 0$; Reset state
1	1	$Q = 1$; Set state

(a) Logic diagram

(b) Function table

Fig. 5-6 D Latch

Application of D Latch

- Output Q is retained until the clock is enabled again, even though the data input is changed

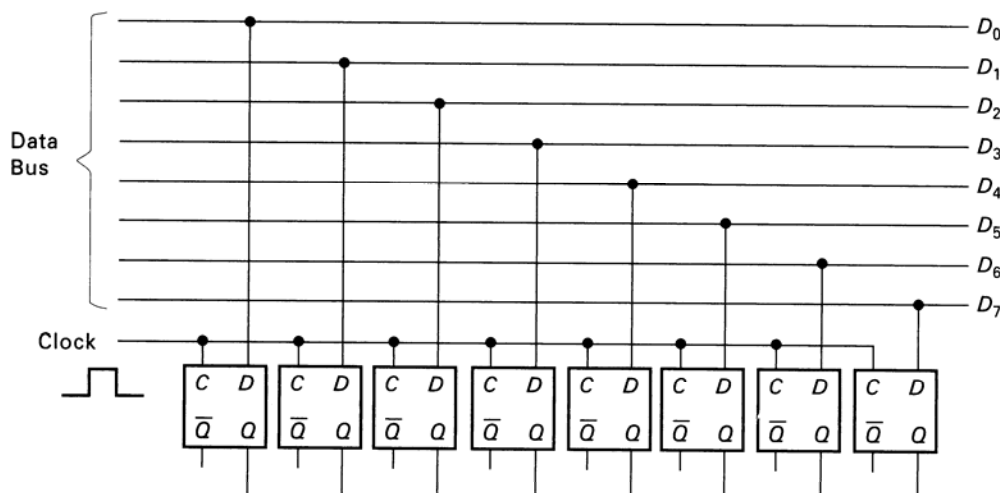
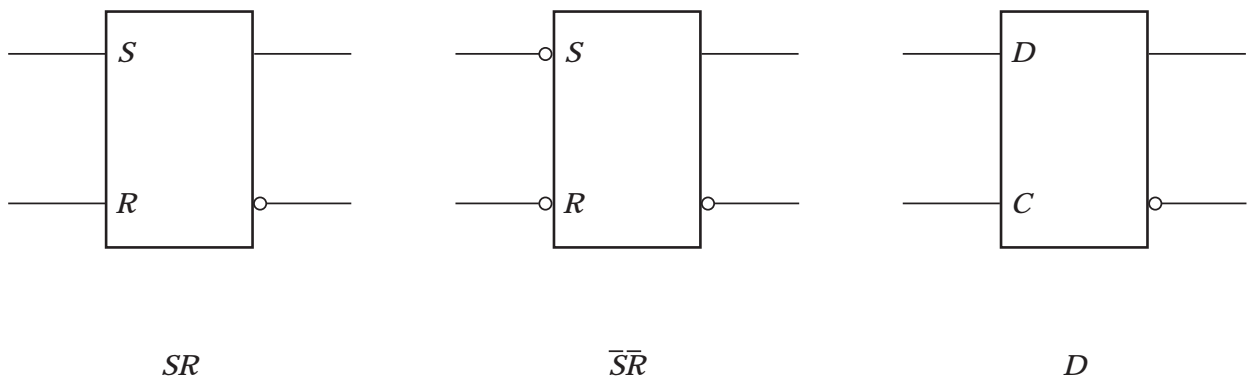


FIGURE 7-27 Computer-output port

Graphic Symbols for Latches



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Flip-Flops

- Latch : output changes as input changes while the clock pulse is in the logic 1, case (a)
 - Unpredictable situation due to continuous state changing
- Flip-flop : output only changes at clock edge

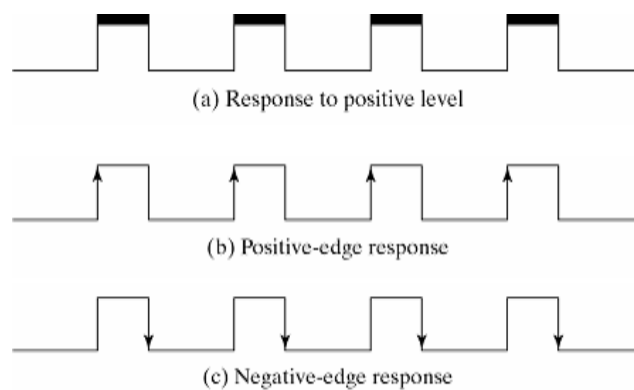


Fig. 5-8 Clock Response in Latch and Flip-Flop

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Master-Slave D Flip-Flop

- Negative edge triggered D flip-flop
 - CLK=0 : master disable, slave enable
 - CLK=1 : master enable, slave disable
- Positive edge triggered D flip-flop
 - Attach inverter on the other way

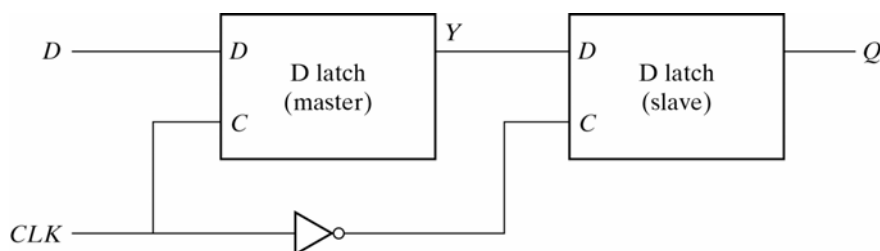


Fig. 5-9 Master-Slave D Flip-Flop

Negative Edge Triggered M-S D Flip-Flop

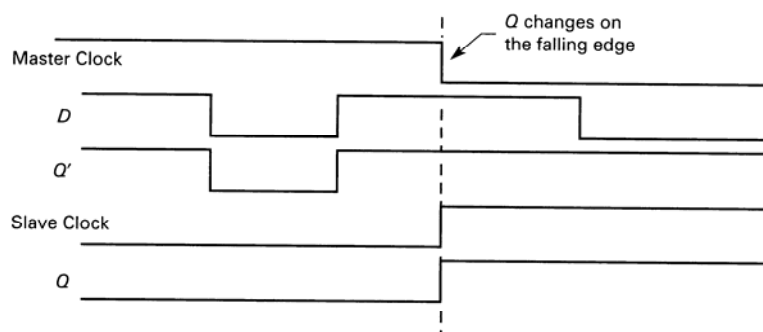
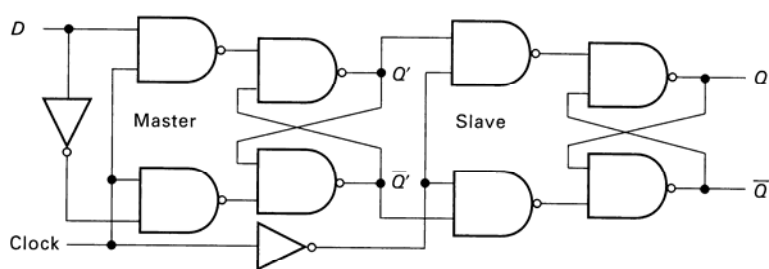


FIGURE 7-31 Negative edge-triggered master-slave D flip-flop

D-type Positive Edge Triggered Flip-Flop

- Consist of 3 SR-latches
- When CLK=0, S=R=1 → state is maintained
- Q changes only when CLK becomes 0 to 1, no change when 1→0
 - If D=0 when CLK→1, R→0 (Reset state, Q=0)
 - If D→1 while CLK=1, R remains at 0
 - CLK→0, R→1, State is maintained
 - If D=1 when CLK→1, S→0 (Set state, Q=1)

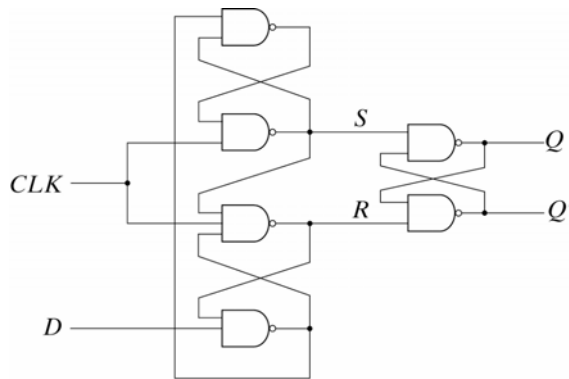


Fig. 5-10 D-Type Positive-Edge-Triggered Flip-Flop

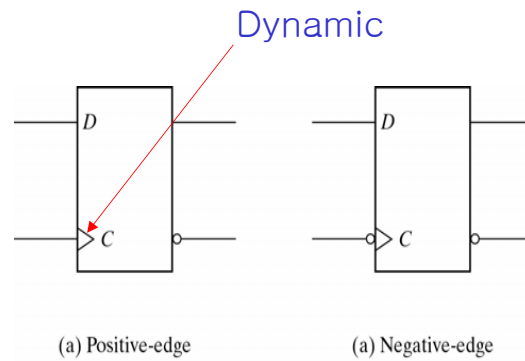


Fig. 5-11 Graphic Symbol for Edge-Triggered D Flip-Flop

D-type Positive Edge Triggered Flip Flop

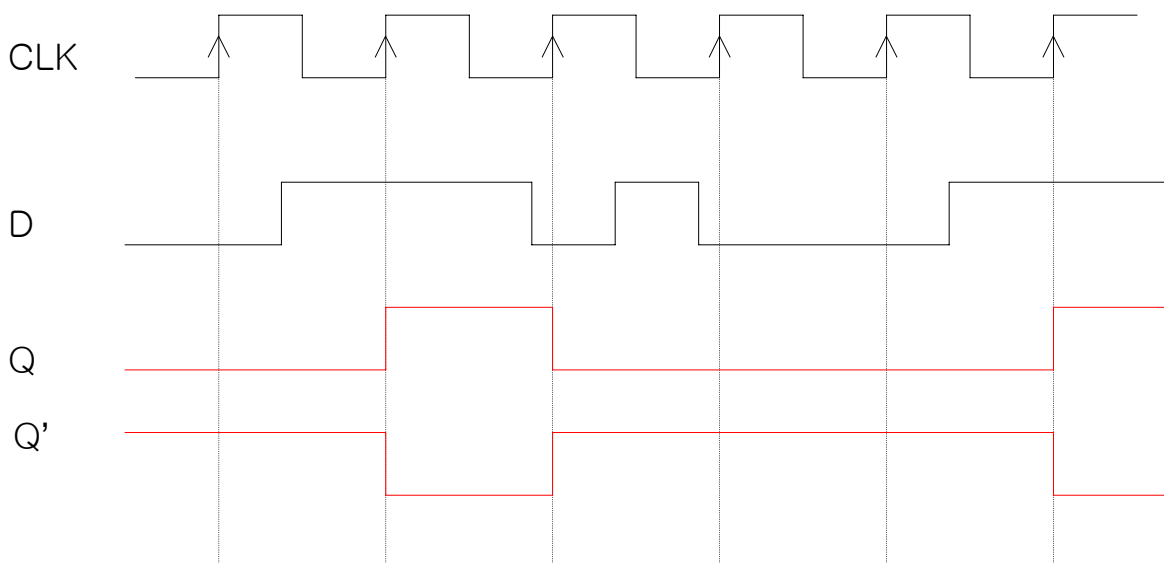


Figure: Positive edge triggered D flip-flop timing diagram

D-type Negative Edge Triggered Flip Flop

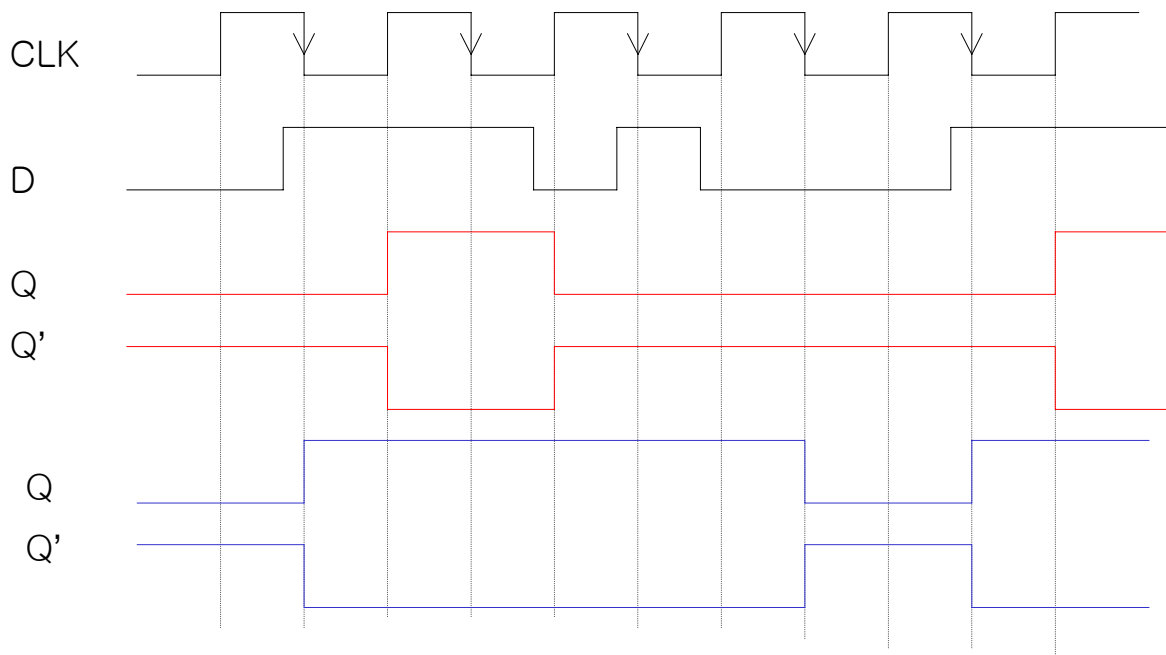
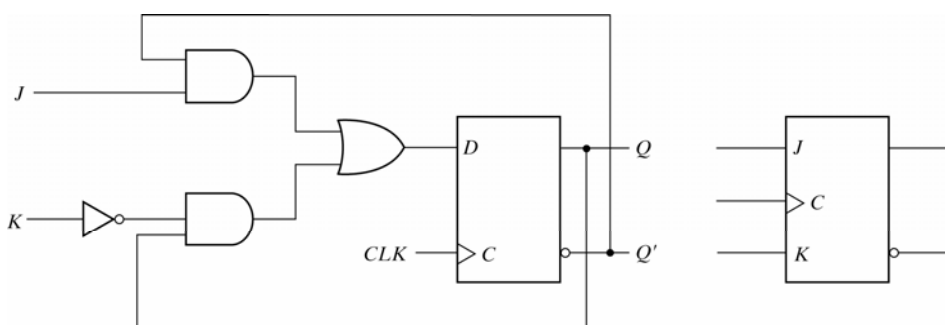


Figure: Negative edge triggered D flip-flop timing diagram

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JK Flip-Flop

- Performs three operations
 - Set($J=1, K=0$), Reset($J=0, K=1$), Complement($J=K=1$)
- $D = JQ' + K'Q$
 - $J=1, K=0$: $D = Q' + Q = 1$ → Sets $Q=1$ at the next clock edge
 - $J=0, K=1$: $D = 0$ → Resets $Q=0$ at the next clock edge
 - $J=K=1$: $D = Q'$ (Complement), $J=K=0$: $D=Q$ (Unchanged)



(a) Circuit diagram

(b) Graphic symbol

Fig. 5-12 JK Flip-Flop

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T Flip-Flop

- Complementing flip-flop
- From D flip-flop
 - $D = TQ' + T'Q$

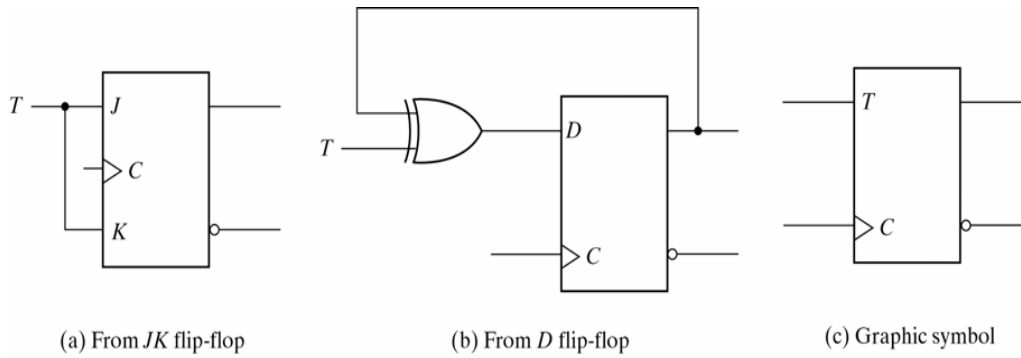


Fig. 5-13 T Flip-Flop

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T Flip-Flop Positive Edge Triggered

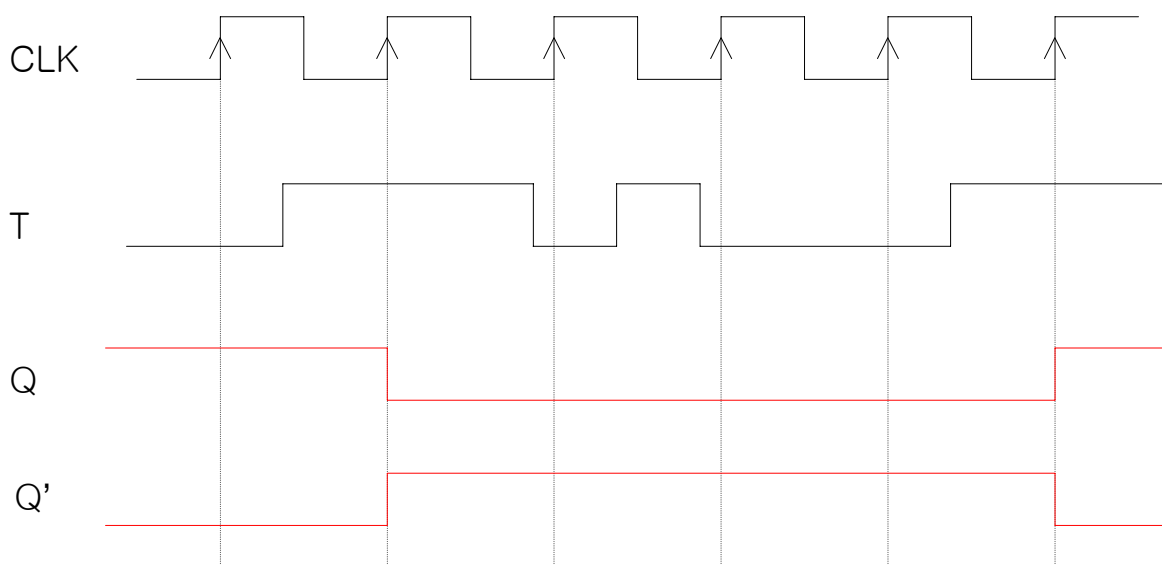


Figure: Positive edge triggered T flip-flop timing diagram

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Characteristic Tables

- Flip-flop characteristic tables
 - $Q(t)$: present state prior to the application of a clock edge
 - $Q(t+1)$: next state one clock period later

Table 5-1
Flip-Flop Characteristic Tables

JK Flip-Flop			
<i>J</i>	<i>K</i>	$Q(t + 1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop		
<i>D</i>	$Q(t + 1)$	
0	0	Reset
1	1	Set

T Flip-Flop			
<i>T</i>	$Q(t + 1)$		
0	$Q(t)$	No change	
1	$Q'(t)$	Complement	

Characteristic Equations

- D-flip flop
 - $Q(t+1)=D$
- J-K flip flop
 - $Q(t+1)=JQ'+K'Q$
- T flip flop
 - $Q(t+1)=TQ'+T'Q$

Table 5-1
Flip-Flop Characteristic Tables

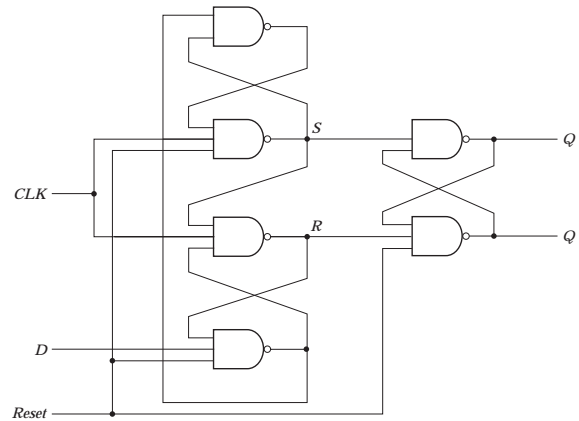
JK Flip-Flop			
<i>J</i>	<i>K</i>	$Q(t + 1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop		
<i>D</i>	$Q(t + 1)$	
0	0	Reset
1	1	Set

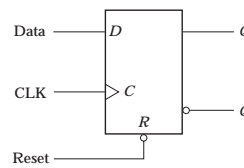
T Flip-Flop			
<i>T</i>	$Q(t + 1)$		
0	$Q(t)$	No change	
1	$Q'(t)$	Complement	

Direct Inputs

- For bringing all flip-flops in the system to a known starting state prior to the clocked operation



(a) Circuit diagram



(b) Graphic symbol

R	C	D	Q	\bar{Q}
0	X	X	0	1
1	\uparrow	0	0	1
1	\uparrow	1	1	0

(b) Function table

Analysis Of Clocked Sequential Circuits

- Behavior of clocked sequential circuit is determined from input, output and present state
- Output and next state are a function of input and present state
- In this section, we introduce an algebraic representation for specifying the next-state condition in terms of the present state and inputs

State Equations (Transition Equations)

- Specifies the next state and output as a function of the present state and inputs

- $A(t+1) = A(t)x(t) + B(t)x(t)$
- $B(t+1) = A'(t)x(t)$
- $y(t) = (A(t) + B(t))x'(t)$

- $t+1$: one clock edge later

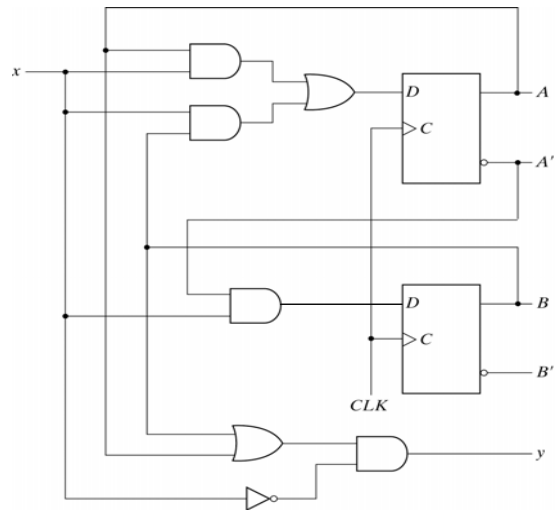


Fig. 5-15 Example of Sequential Circuit

State Table (Transition Table)

- Time sequence of inputs, outputs, and flip-flop states
- Two types of state table exist
- One form may be preferable over the other, depending on the application

Table 5-2
State Table for the Circuit of Fig. 5-15

Present State		Input x	Next State		Output y
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Table 5-3
Second Form of the State Table

Present State AB	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
	AB	AB	y	y
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0
11	00	10	1	0

State Diagram

- A kind of flow diagram
- Can be derived from state table
 - State-circle, transition-line, I/O

Table 5-2
State Table for the Circuit of Fig. 5-15

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

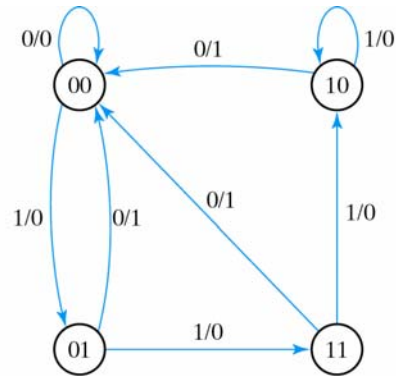
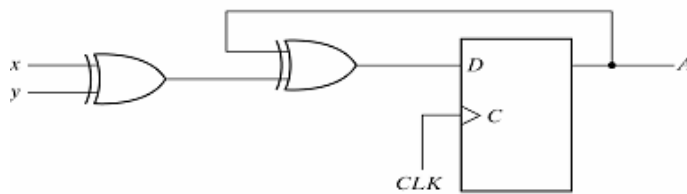


Fig. 5-16 State Diagram of the Circuit of Fig. 5-15

Analysis with D Flip-Flops

- Input equation : $D_A = A \oplus x \oplus y$
 - D flip-flop with output A
- State equation is equal to input equation

$$A(t+1) = A \oplus x \oplus y$$



(a) Circuit diagram

Present state	Inputs		Next state
A	x	y	A
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table



(c) State diagram

Fig. 5-17 Sequential Circuit with D Flip-Flop

No output, slash is not needed

Analysis with JK Flip-Flops

- State equation is not the same as the input equation
- Have to refer characteristic table or characteristic equation
- Flip-flop Input equations

$$J_A = B \quad K_A = Bx'$$

$$J_B = x' \quad K_B = A'x + Ax' = A \oplus B$$

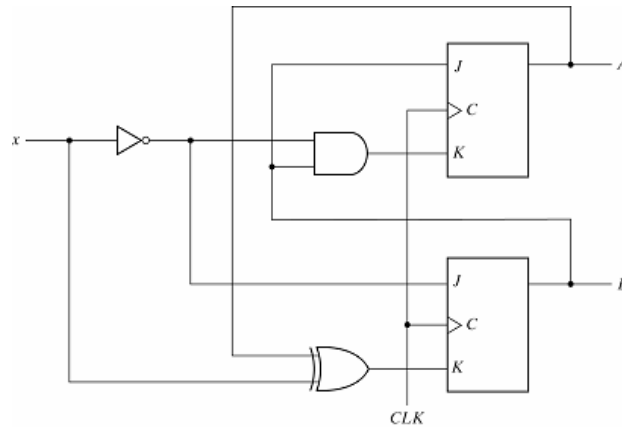


Fig. 5-18 Sequential Circuit with JK Flip-Flop

Analysis with JK Flip-Flops

- State table and state diagram

Table 5-4
State Table for Sequential Circuit with JK Flip-Flops

Present State		Input	Next State		Flip-Flop Inputs			
A	B		A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

$$A(t+1) = JA' + K'A$$

$$B(t+1) = JB' + K'B$$

$$A(t+1) = BA' + (Bx')'A = A'B + AB' + Ax$$

$$B(t+1) = x'B' + (A \oplus x)'B = B'x' + ABx + A'Bx'$$

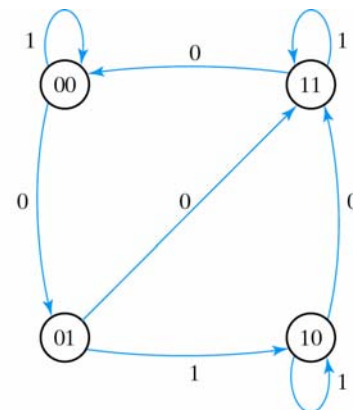


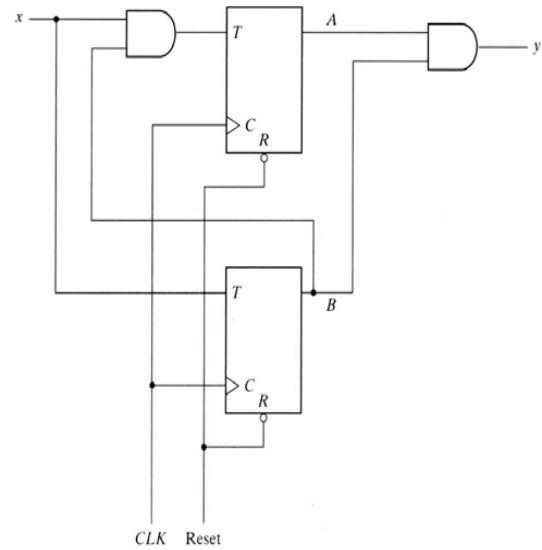
Fig. 5-19 State Diagram of the Circuit of Fig. 5-18

Analysis with T Flip-Flops

- Input equations and output equation
 $T_A = Bx$, $T_B = x$
 $y = AB$
- State equations are derived from characteristic equation

$$A(t+1) = (Bx)'A + (Bx)A' = AB' + Ax' + A'Bx$$

$$B(t+1) = x \oplus B$$

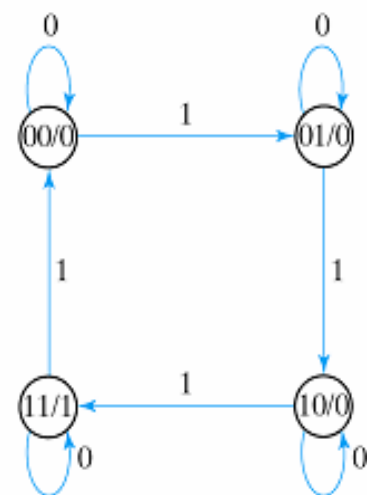


(a) Circuit diagram

Analysis with T Flip-Flops

Table 5-5
State Table for Sequential Circuit with T Flip-Flops

Present State		Input	Next State		Output
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1



(b) State diagram

State/output

Input

Example

- A sequential circuit with two D flip-flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations:

$$A(t+1) = x'y + xA(t)$$

$$B(t+1) = x'B(t) + xA(t)$$

$$Z = B(t)$$

- (a) Draw the logic diagram of the circuit.
- (b) List the state table for the sequential circuit.
- (c) Draw the corresponding state diagram.

Mealy and Moore Models

- Mealy model : output is a function of the present state and input
 - Inputs must be synchronized with the clock
 - Outputs must be sampled at the clock edge
- Moore model : output is a function of the present state only
 - Outputs are synchronized with the clock

Design Procedure

- Sequential circuit design: requires state table
 - ⇔ Combinational circuit : truth table
- The number of flip-flop is determined from the number of states in circuit
 - If 2^n states exist, there are n flip-flops
- Once the type and number of flip-flops are determined
 - Sequential circuit problem is transformed into a combinational circuit problem

Design Procedure

- Design steps
 - 1) Derive a state diagram or state table
 - 2) Reduce the number of states if necessary
 - 3) Assign binary values to the states
 - 4) Obtain the binary-coded state table
 - 5) Choose the type of flip-flops to be used
 - 6) Derive the flip-flop input equations and output equations
 - 7) Draw the logic diagram

Derive a State Diagram

- Sequential detector
 - Three or more consecutive 1's in a string of bits coming through an input line

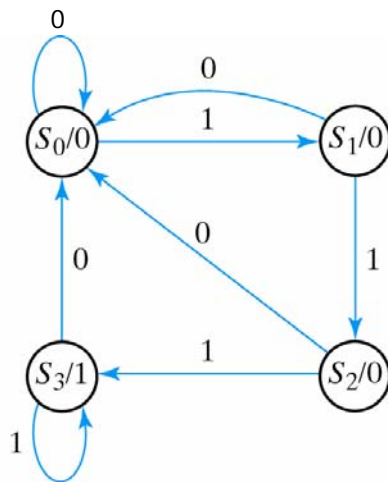
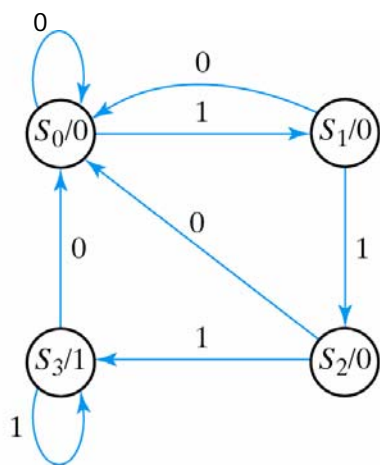


Fig. 5-24 State Diagram for Sequence Detector

Assign Binary Values To The States



- State Assign as followings
- 4 States → 2 bit assign
 - S0 = 00
 - S1 = 01
 - S2 = 10
 - S3 = 11

Fig. 5-24 State Diagram for Sequence Detector

Obtain The Binary-coded State Table

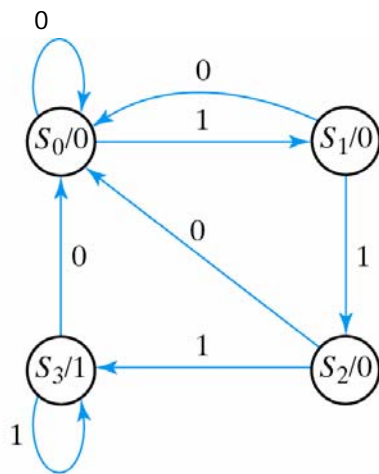


Table 5-11
State Table for Sequence Detector

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	1	1

Fig. 5-24 State Diagram for Sequence Detector

Synthesis using D Flip-Flops

- Input equations are obtained directly from the next states

Table 5-11
State Table for Sequence Detector

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	1	1

$$A(t+1) = D_A(A, B, x) = \sum(3,5,7)$$

$$B(t+1) = D_B(A, B, x) = \sum(1,5,7)$$

$$y(A, B, x) = \sum(6,7)$$

Draw the Logic Diagram

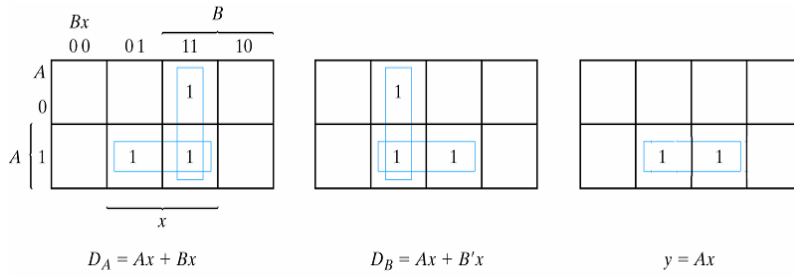


Fig. 5-25 Maps for Sequence Detector

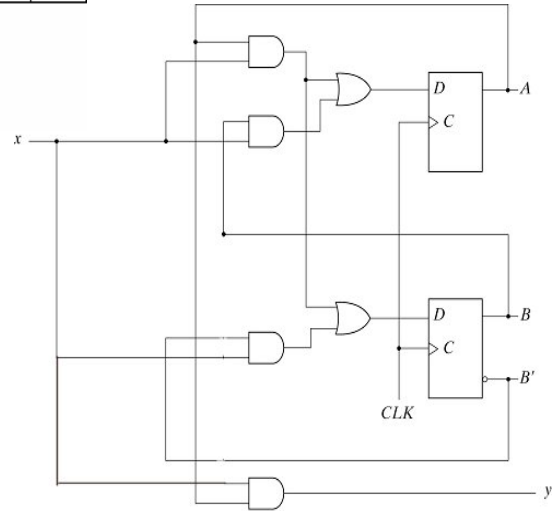


Fig. 5-26 Logic Diagram of Sequence Detector

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Excitation Table

Q(t)	Q(t+1)	J	K	Q(t)	Q(t+1)	T
0	0	0	X	0	0	0
0	1	1	X	0	1	1
1	0	X	1	1	0	1
1	1	X	0	1	1	0

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Synthesis with JK Flip-Flops

- Input equations evaluated from the present state to next state transition

Table 5-13
State Table and JK Flip-Flop Inputs

Present State		Input	Next State		Flip-Flop Inputs			
A	B		A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Synthesis using JK Flip-Flops

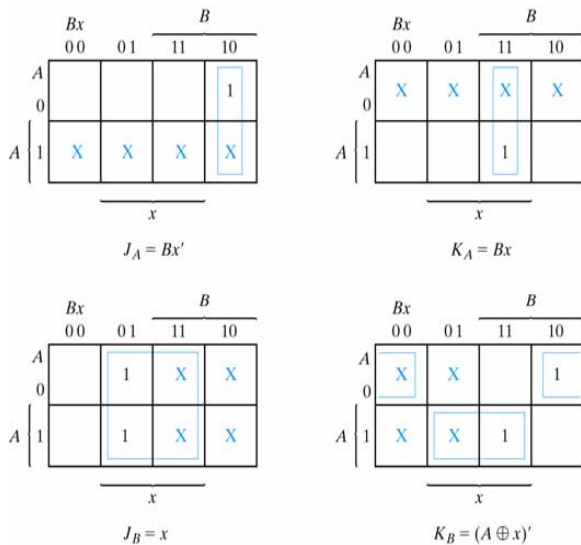


Fig. 5-27 Maps for J and K Input Equations

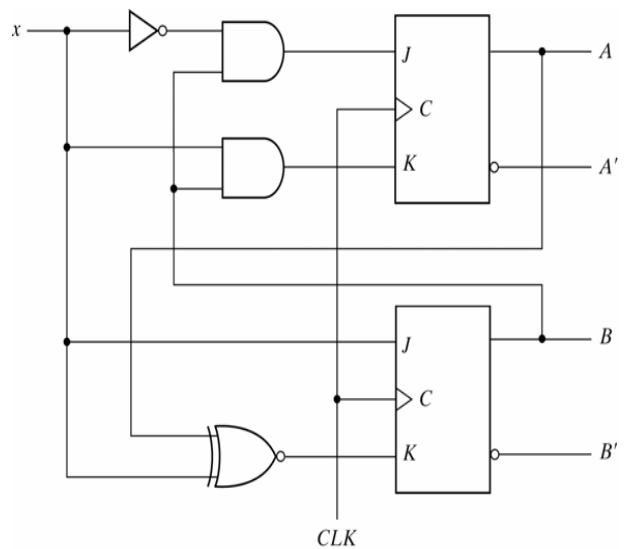


Fig. 5-28 Logic Diagram for Sequential Circuit with JK Flip-Flops

Example

- Synthesis using T flip-flops
 - Design with T flip-flops

Synthesis using T flip-flops

- 3-bit binary counter
 - 3-bit counter has 3 flip-flops and can count from 0 to $2^n - 1$ ($n=3$)

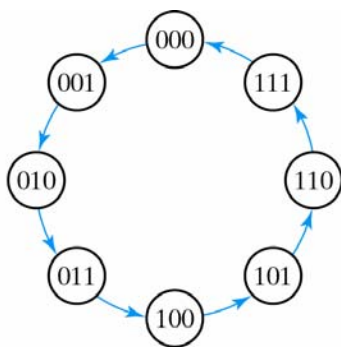


Fig. 5-29 State Diagram of 3-Bit Binary Counter

Table 5-14
State Table for 3-Bit Counter

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Synthesis using T Flip-Flops

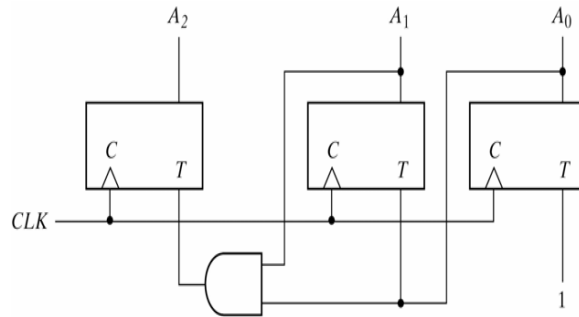
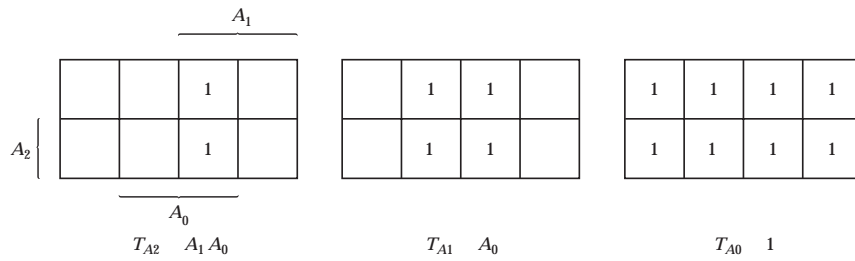


Fig. 5-31 Logic Diagram of 3-Bit Binary Counter

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Example

1. Synthesis the 3-bit binary counter using D flip-flop
2. Synthesis the 3-bit binary counter using J-K flip-flop

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