1. Design a combinational circuit that generates the 9’s complement of a BCD digit using the unused combinations of the code as don’t-care conditions. For example, 9’s complement of “0001” is “1000”. (20pt)

2. Design the negative edge triggered synchronous 3-bit binary counter using T flip-flops and one input $x$, count up when $x=0$, and count down when $x=1$. (20pt)

3. Design a positive edge triggered synchronous sequential circuit with two JK flip-flops A and B and two inputs $x$ and $y$. if $x=0$, the circuit remains in the same state regardless of the value of $y$. when $x=1$ and $y=1$, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When $x=1$ and $y=0$, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeat. (20pt)

4. Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. And obtain the next number when it start at 2, 5 (20pt)

5. Fill out three blanks with proper VHDL codes. (20pt)
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY EX_5_3_V IS
  PORT(
    RST, SI, CLK : IN STD_LOGIC;
    REG        : OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
END EX_5_3_V;

ARCHITECTURE BF OF EX_5_3_V IS
  SIGNAL SR : (                      )
  (__________) DIFF_RST
    PORT(  D, RST, CLK : IN STD_LOGIC;
           Q          : OUT STD_LOGIC);
END COMPONENT;

BEGIN
  DF7 : DIFF_RST PORT MAP(SI, RST, CLK, SR(7));
  DF6 : DIFF_RST PORT MAP(SR(7), RST, CLK, SR(6));
  DF5 : DIFF_RST PORT MAP(SR(6), RST, CLK, SR(5));
  DF4 : DIFF_RST PORT MAP(SR(5), RST, CLK, SR(4));
  DF3 : DIFF_RST PORT MAP(SR(4), RST, CLK, SR(3));
  DF2 : DIFF_RST PORT MAP(SR(3), RST, CLK, SR(2));
  DF1 : DIFF_RST PORT MAP(SR(2), RST, CLK, SR(1));
  DF0 : DIFF_RST PORT MAP(SR(1), RST, CLK, SR(0));
  REG <= SR;
END BF;

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DIFF_RST IS
  PORT(
    D, RST, CLK : IN STD_LOGIC;
    Q          : OUT STD_LOGIC);
END DIFF_RST;

ARCHITECTURE BF OF DIFF_RST IS
BEGIN
  PROCESS(RST, CLK)
  BEGIN
    IF RST = '0' THEN Q <= '0';
    ELSIF (__________) THEN Q <= D;  --when rising edge
    END IF;
  END PROCESS;
END BF;