1. Design a 4-input priority encoder with input D0 (the Lowest Significant Bit) having the highest priority and input D3 (the Highest Significant Bit) having the lowest priority. Assume that x, y are outputs, and y is the Lowest Significant Bit. Don’t care the outputs when all 4-inputs are zero. (20pt)

2. Design the negative edge triggered synchronous 3-bit binary counter using D flip-flops and one input x, count up when x=1, and count down when x=0. (20pt)

3. Explain functions of the following logic when the inputs to the MUX change. (20pt)

4. Fill out three blanks with proper VHDL codes. (20pt)

5. Obtain the input Boolean functions for a synchronous counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use JK flip-flops. And obtain the next number when it start at 3, 5 or 7 (20pt)
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY EX_5_3_V IS
  PORT(
    RST, SI, CLK : IN STD_LOGIC;
    REG         : OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
END EX_5_3_V;

ARCHITECTURE BF OF EX_5_3_V IS
  SIGNAL SR : (                       )
  (________) DIFF_RST
  PORT(
    D, RST, CLK : IN STD_LOGIC;
    Q           : OUT STD_LOGIC);
END COMPONENT;

BEGIN
  DF7 : DIFF_RST PORT MAP(SI, RST, CLK, SR(7));
  DF6 : DIFF_RST PORT MAP(SR(7), RST, CLK, SR(6));
  DF5 : DIFF_RST PORT MAP(SR(6), RST, CLK, SR(5));
  DF4 : DIFF_RST PORT MAP(SR(5), RST, CLK, SR(4));
  DF3 : DIFF_RST PORT MAP(SR(4), RST, CLK, SR(3));
  DF2 : DIFF_RST PORT MAP(SR(3), RST, CLK, SR(2));
  DF1 : DIFF_RST PORT MAP(SR(2), RST, CLK, SR(1));
  DF0 : DIFF_RST PORT MAP(SR(1), RST, CLK, SR(0));
  REG <= SR;
END BF;

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DIFF_RST IS
  PORT(
    D, RST, CLK : IN STD_LOGIC;
    Q           : OUT STD_LOGIC);
END DIFF_RST;

ARCHITECTURE BF OF DIFF_RST IS
BEGIN
  PROCESS(RST, CLK)
  BEGIN
    IF RST = '0' THEN Q <= '0';
    ELSIF (______________) THEN Q <= D; --when rising edge
    END IF;
  END PROCESS;
END BF;