

디지털 공학 (MEC520)  
Midterm Examination

Spring, 2005

1. Perform the following subtraction using the 2's complement after converting the decimal numbers to binary numbers. (8 pt)

$$36 - 63.6875$$

2. Reduce the following Boolean expression to the indicated number of literals. (8 pt each)

a)  $(x'y' + z)' + z + xy + wz$  to three literals

b)  $A'B(D' + C'D) + B(A + A'CD)$  to one literal

3. Simplify the following Boolean functions by first finding the essential prime implicants. (8 pt each)

a)  $F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$

b)  $F(A, B, C, D) = \Sigma(1, 3, 4, 5, 9, 10, 11, 12, 13, 14, 15)$

4. Simplify the following functions in product of sums. (8 pt each)

a)  $F(w, x, y, z) = \Sigma(0, 2, 5, 7, 8, 10)$

b)  $F(A, B, C, D) = \Pi(1, 3, 5, 7, 13, 15)$

c)  $F(x, y, z) = x'z' + y'z' + yz' + xy$

5. Simplify the following Boolean Function F, together with the don't care conditions d, and then express the simplified function in sum of minterms. (8 pt each)

a)  $F(A, B, C, D) = \Sigma(0, 6, 8, 13, 14)$

d)  $d(A, B, C, D) = \Sigma(2, 4, 10)$

b)  $F(A, B, C, D) = \Sigma(1, 3, 5, 7, 9, 15)$

d)  $d(A, B, C, D) = \Sigma(4, 6, 12, 13)$

6. Convert the logic diagram of the circuit shown in Fig. 1 into a multiple-level NAND circuit. (12 pt)

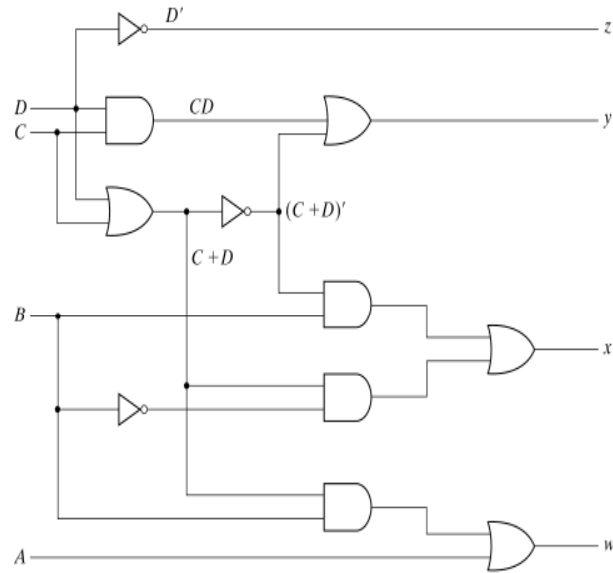


Fig. 1 Logic Diagram for BCD to Excess-3 Code Converter

7. Implement the following Boolean expression with exclusive-OR and AND gates. (8 pt)

$$F = AB'CD' + A'BCD' + AB'C'D + A'BC'D$$

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